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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,910	04/16/2004	Byung Tai Do	27-017	8877

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,910	DO ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/04 and 07/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 04/16/2004 is acceptable.

Claim Rejections § 102 & § 103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 5-7, 10-12, 15-17, and 20 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Akram U.S. Patent 5,904,497 (the '497 patent).

The '497 patent discloses in Figures 1-7, particularly Fig. 7, and respective portions of the specification a semiconductor package and a method of assembling thereof as claimed or substantially as claimed.

Referring to **claims 1, 6, 11, and 16**, the '497 patent discloses a method of assembling a semiconductor package and the resulting semiconductor package with stacked dies comprising:

providing a substrate ("printed circuit board" 10);

attaching a first die (14) to the substrate;

electrically connecting the first die to the substrate;

attaching a surface plate 18 having an undercut around its periphery to the first die;

attaching a second die to the surface plate;

electrically connecting the second die to the substrate; and

encapsulating the first die, the surface plate, and the second die.

However, the reference fails to disclose that the surface plate 18 functions as a heat sink as claimed.

Nevertheless, the surface plate 18 is disclosed as being formed of ceramic or silicon (column 3, lines 54-55) which "have the advantage of a matched coefficient of thermal expansion with the silicon of the die to which it will be attached" and wherein the "[T]hermal matching reduces failures of the die resulting from uneven expansion during thermal cycling" (column 6, lines 44-48). Therefore, it appears that the surface plate 18 functions as a heat sink because it matches the thermal state of the die.

Referring to **claims 2, 7, 12, and 17**, as evident from Fig. 7, the reference further discloses electrically connecting the first die to the substrate uses a number of bonding wires (12)

and attaching a heat sink attaches a heat sink that extends laterally over the number of bonding wires.

Referring to **claims 5 and 15**, as evident from Fig. 7, the reference further discloses attaching a heat sink attaches a heat sink that extends laterally beyond the edges of the second die.

Referring to **claims 10 and 20**, the reference further discloses providing a heat sink attaches a heat sink between each adjoining pair of dies in the stack of dies (column 5, lines 57-63).

Claim Rejections § 102

3. **Claims 1-2, 5-7, 10-12, 15-17, and 20** are rejected under 35 U.S.C. 102(b) as being anticipated by Akram U.S. Patent 6,351,028 (the '028 patent).

The '028 patent discloses in Figures 2-9, particularly Fig. 7, and respective portions of the specification a semiconductor package, a method of using, and a method of assembling thereof as claimed.

Referring to **claims 1, 6, 11, and 16**, the '028 patent discloses a method of assembling a semiconductor package and the resulting semiconductor package with stacked dies comprising:

providing a substrate (22);

attaching a first die (24) to the substrate;

electrically connecting the first die to the substrate;

attaching a heat sink (26, column 3, lines 61-67, "transfer of thermal energy or heat from semiconductor devices in contact with or around T-interposer 26") having an undercut around its periphery to the first die;

attaching a second die to the heat sink;

electrically connecting the second die to the substrate; and

encapsulating (Fig. 7, using epoxy 50) the first die, the heat sink, and the second die.

Referring to **claims 2, 7, 12, and 17**, as evident from the figures, the reference further discloses electrically connecting the first die to the substrate uses a number of bonding wires (no number) and attaching a heat sink attaches a heat sink that extends laterally over the number of bonding wires.

Referring to **claims 5 and 15**, as evident from Figs. 5 and 9, the reference further discloses attaching a heat sink attaches a heat sink that extends laterally beyond the edges of the second die.

Referring to **claims 10 and 20**, as evident from Fig. 7, the reference further discloses providing a heat sink attaches a heat sink between each adjoining pair of dies in the stack of dies.

4. **Claims 1-2, 5-7, 11-12, and 15-17** are rejected under 35 U.S.C. 102(e) as being anticipated by Fan U.S. Patent 6,818,978 (the '978 patent).

The '978 patent discloses in Fig. 1 and respective portions of the specification a semiconductor package, a method of using, and a method of assembling thereof as claimed.

Referring to **claims 1, 6, 11, and 16**, the '978 patent discloses a method of assembling a semiconductor package and the resulting semiconductor package with stacked dies comprising:

providing a substrate (22);

attaching a first die (28) to the substrate;

electrically connecting the first die to the substrate;

attaching a heat sink (40/32, "spacer" and "shield", column 3, lines 28-34, and note that the spacer/shield could be a single-piece T-shaped unitary metal piece – hence would function as and properly labeled a heat sink (column 6, lines 46-50) having an undercut around its periphery to the first die;

attaching a second die (30) to the heat sink;

electrically connecting the second die to the substrate; and

encapsulating (Fig. 7, using encapsulating material 36) the first die, the heat sink, and the second die.

Referring to **claims 2, 7, 12, and 17**, as evident from the figure, the reference further discloses electrically connecting the first die to the substrate uses a number of bonding wires (34) and attaching a heat sink attaches a heat sink that extends laterally over the number of bonding wires.

Referring to **claims 5 and 15**, as evident from Fig. 1, the reference further discloses attaching a heat sink attaches a heat sink that extends laterally beyond the edges of the second die.

Claim Rejections § 103

5. **Claims 3, 8, 13, and 18** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '028 patent in view of Chiu et al. U.S. Patent 6,437,984 (the '984 patent).

The '028 patent discloses a semiconductor package with stacked dies and a method of assembling and using thereof as claimed and as detailed above for claims 1, 6, 11, and 16, but fails to disclose that the heat sink is electrically grounded. The '984 patent, in disclosing a thermally enhanced chip scale package having a heat sink (114, Fig. 1B), teaches that the heat sink may be wire bonded to a ground connection to provide the packaged integrated circuit with shielding from electrical or electromagnetic interference (column 2, lines 16-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '028 patent package's heat sink so that the heat sink is electrically grounded using wire bonding. One would have been motivated to make such a modification in view of the teachings by the '984 patent that ground connection using wire bonding provide the packaged integrated circuit with shielding from electrical or electromagnetic interference.

6. **Claims 4, 9, 14, and 19** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '028 patent in view of the '984 patent and further in view of Shin et al. U.S. Patent 5,854,511 (the '511 patent).

The '028 patent discloses a semiconductor package with stacked dies and a method of assembling and using thereof as claimed and as detailed above for claims 1, 6, 11, and 16, but fails to disclose that the heat sink is electrically grounded and thus further fails to disclose that the heat sink has an electrically conductive coating connected to a ground plane on the substrate and consequently the second die fails to be connected to the electrically conductive coating.

However, as detailed above, one of ordinary skill in the art at the time the invention was made would include bonding wire grounding to the substrate to shield the package from electrical or electromagnetic interference.

Nevertheless, even with this modification, the heat sink of the modified package lacks an electrically conductive coating and thus lacks an electrically conductive coating connected to a ground plane on the substrate.

The '511 patent, in disclosing a semiconductor package including a multilayered heat sink, teaches in the Abstract, Figs. 1 and 2, and column 1, lines 10-22, that an electrically conductive coating formed of silver or nickel and palladium as part of the heat sink results in an improvement in performance of the finally produced semiconductor package.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '028 patent modified in view of the '984 patent as detailed above for shielding from electrical or electromagnetic interference such that the heat sink has an electrically conductive coating. One would have been motivated to make such a modification in view of the teachings by the '511 patent that an electrically conductive coating formed of silver or nickel and palladium as part of the heat sink results in an improvement in performance of the finally produced semiconductor package. Thus the final modified package would have a heat sink having an electrically conductive coating connected to a ground plane on the substrate and that the second die would be connected to the electrically conductive coating as the second die is connected to the heat sink which has the electrically conductive coating.

7. **Claims 3, 8, 13, and 18** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '978 patent in view of the '984 patent.

The '978 patent discloses a semiconductor package with stacked dies and a method of assembling and using thereof as claimed and as detailed above for claims 1, 6, 11, and 16, but fails to disclose that the heat sink is electrically grounded. The '984 patent, in disclosing a thermally enhanced chip scale package having a heat sink (114, Fig. 1B), teaches that the heat sink may be wire bonded to a ground connection to provide the packaged integrated circuit with shielding from electrical or electromagnetic interference (column 2, lines 16-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '978 patent package's heat sink so that the heat sink is electrically grounded using wire bonding. One would have been motivated to make such a modification in view of the teachings by the '984 patent that ground connection using wire bonding provide the packaged integrated circuit with shielding from electrical or electromagnetic interference.

8. **Claims 4, 9, 14, and 19** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '978 patent in view of the '984 patent and further in view of the '511 patent.

The '978 patent discloses a semiconductor package with stacked dies and a method of assembling and using thereof as claimed and as detailed above for claims 1, 6, 11, and 16, but fails to disclose that the heat sink is electrically grounded and thus further fails to disclose that the heat sink has an electrically conductive coating connected to a ground plane on the substrate and consequently the second die fails to be connected to the electrically conductive coating.

However, as detailed above, one of ordinary skill in the art at the time the invention was made would include bonding wire grounding to the substrate to shield the package from electrical or electromagnetic interference.

Nevertheless, even with this modification, the heat sink of the modified package lacks an electrically conductive coating and thus lacks an electrically conductive coating connected to a ground plane on the substrate.

The '511 patent, in disclosing a semiconductor package including a multilayered heat sink, teaches in the Abstract, Figs. 1 and 2, and column 1, lines 10-22, that an electrically conductive coating formed of silver or nickel and palladium as part of the heat sink results in an improvement in performance of the finally produced semiconductor package.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '978 patent modified in view of the '984 patent as detailed above for shielding from electrical or electromagnetic interference such that the heat sink has an electrically conductive coating. One would have been motivated to make such a modification in view of the teachings by the '511 patent that an electrically conductive coating formed of silver or nickel and palladium as part of the heat sink results in an improvement in performance of the finally produced semiconductor package. Thus the final modified package would have a heat sink having an electrically conductive coating connected to a ground plane on the substrate and that the second die would be connected to the electrically conductive coating as the second die is connected to the heat sink which has the electrically conductive coating.

9. **Claims 10 and 20** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '978 patent.

The '978 patent discloses a semiconductor package with stacked dies and a method of assembling and using thereof as claimed and as detailed above for claims 6 and 16, but fails to disclose that providing a heat sink attaches a heat sink between each adjoining pair of dies in the stack of dies. In other words, the '978 patent discloses providing a heat sink attaches a heat sink between the only adjoining pair of dies in the stack of dies shown in Fig. 1 rather than providing a heat sink attaches a heat sink between each adjoining pair of dies in the stack of dies. Nevertheless, because the reference also fails to disclose that the pair of dies is the only pair, it would appear that the package could be modified to include more heat sinks and more dies on the depicted pair of dies, a task that one of ordinary skill in the art at the time the invention was made could easily perform and therefore would have been obvious. A package such modified would comprise a heat sink between each adjoining pair of dies in the stack of dies.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
January 24, 2005